CLAIMS:

What is claimed is:

1. A comparator circuit, comprising:

a pair of differential inputs for receiving a differential signal pair;

a single-ended input for receiving a single-ended signal;

a reference combiner, whereby a reference for detecting said single-ended signal is derived in conformity with both signals of said differential signal pair; and

a single-ended comparator for comparing said single-ended input with said reference, whereby said single-ended signal is detected in conformity with said differential signal pair.

2. The comparator circuit of Claim 1, wherein said reference combiner comprises:

a first controlled current source having an input coupled to a first signal of said differential signal pair;

a second controlled current source having an input coupled to a second signal of said differential signal pair; and

a current summing junction for summing an output of said first controlled current source and an output of said second controlled current source for providing said reference.

3. The comparator circuit of Claim 2, wherein said single-ended comparator comprises a third controlled current source having an input coupled to said single-ended input and an output coupled to said current summing junction for comparing said single-ended signal to said reference.

4. The comparator circuit of Claim 3, wherein said first controlled current source comprises a first transistor having a gate coupled to said first signal of said differential signal pair, wherein said second controlled current source comprises a second transistor having a gate coupled to said second signal of said differential signal pair, and wherein said third controlled current source comprises a third transistor having a gate coupled to said single-ended input.

5. The comparator circuit of Claim 4, further comprising a fixed current source coupled to said current summing junction, whereby said comparator detects a difference between said single-ended signal and an average of said first signal and said second signal of said differential signal pair.

6. The comparator circuit of Claim 4, further comprising a first resistance coupled to a second channel connection of said third transistor, whereby a gain of a singlential output of said comparator is determined.

7. The comparator circuit of Claim 6, further comprising a differential comparator circuit for comparing said pair of differential inputs, said differential comparator circuit comprising a fourth transistor having a gate coupled to said first signal of said differential signal pair, a fifth transistor having a gate coupled to said second signal of said differential signal pair and a first channel connection coupled to a second resistance for providing active mode operation, a second current source coupled to a channel connection of said fourth transistor and a second channel connection of said fifth transistor, whereby said differential comparator detects a difference between said first signal and said second signal of said differential signal pair, and wherein said first resistance has a resistance value twice that of said second resistance, whereby a gain of said active mode of said differential comparator is equal to a gain of said single-ended comparator.

8. The comparator circuit of Claim 2, wherein said first controlled current source comprises a first transistor having a gate coupled to said first signal of said differential signal pair, and wherein said second controlled current source comprises a second transistor having a gate coupled to said second signal of said differential signal pair.

9. The comparator circuit of Claim 8, further comprising a fixed current source coupled to said current summing junction, whereby said reference combiner supplies a current in conformity with an average of said non-inverted signal and said inverted signal of said differential signal pair to said fixed current source.

10. A method for detecting a single-ended signal, said method comprising:

receiving a single-ended signal;

receiving a differential signal pair;

combining both signals of said differential signal pair to provide a reference; and

comparing said single-ended signal to said reference, whereby said single-ended signal is detected in conformity with said differential signal pair.

11. The method of Claim 10, wherein said combining comprises:

controlling a first controlled current source with a first signal of said differential signal pair;

controlling a second controlled current source with a second signal of said differential signal pair; and

summing an output of said first controlled current source and an output of said second controlled current source to provide said reference.

12. The method of Claim 11, wherein said comparing comprises controlling a third controlled current source with said single-ended signal, and wherein said summing further sums an output of said third controlled current source.

13. The method of Claim 12, wherein said summing further sums a current supplied by a fixed current source, whereby said comparing detects a difference between said single-ended signal and an average of said first signal and said second signal of said differential signal pair.

14. The method of Claim 12, further comprising converting a current result of said summing to a voltage via a first resistance, whereby said comparing is performed in an active mode, producing a voltage substantially linearly proportional to a difference between said reference and said single-ended signal in a region where said reference and said single-ended signal are substantially equal.

15. The method of Claim 14, further comprising second comparing said pair of differential inputs to each other to provide a differential pair detected output, wherein said second comparing produces a second voltage via converting a difference current to said second voltage via a second resistor, and wherein said first resistor has a resistance substantially twice that of said second resistor, whereby a gain of said first comparing and a gain of said second comparing are substantially equal.

16. A comparator circuit, comprising:

a pair of differential inputs for receiving a differential signal pair;

a single-ended input for receiving a single-ended signal;

a first transistor having a gate coupled to a first signal of said differential signal pair;

a second transistor having a gate coupled to a second signal of said differential signal pair;

a third transistor having a gate coupled to said single-ended input; and

a fixed current source coupled to a common connection of a first channel connection of each of said first transistor, said second transistor and said third transistor, whereby said single-ended signal is compared to a common-mode value of said differential signal pair.

17. The comparator circuit of Claim 16, further comprising a first resistance coupled to a second channel connection of said third transistor, whereby a first gain of a single-ended output of said comparator is determined in an active region of operation.

18. The comparator circuit of Claim 17, further comprising:

a fourth transistor having a gate coupled to said first signal of said differential signal pair;

a fifth transistor having a gate coupled to said second signal of said differential signal pair;

a second fixed current source coupled to a common connection of a first channel connection of each of said fourth transistor and said fifth transistor, whereby said first signal and said second signal of said differential signal pair are compared; and

a second resistance coupled to a second channel connection of said fifth transistor, whereby a gain of a differential output of said comparator is determined, and wherein a resistance value of said first resistance is substantially twice a resistance value of said second resistance, whereby said first gain is equal to a second gain of said differential output in an active region of operation.